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|---|---|
| MERED, HABTE | |

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| 2616 | |

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/081,748 | BEVERLY ET AL. | |
| | Examiner | Art Unit | |
| | Habte Mered | 2616 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's request filed on 11/20/2006 for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

2. Claims 1-55 remain pending.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claim 37 recites the limitation "said first and second registers" in the first line of the claim. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1, 2, 10-13, 15, 17, and 19-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Kincaid (US 6, 640, 275).

*Kincaid teaches system and method for data transfer between buses having different speeds.*

7. Regarding **claims 1 and 11**, Kincaid teaches a method and device comprising: receiving a data frame of a first size **(See Figure 5, from ingress data 500 frames of 32 bits enter demux 505)**; demultiplexing the data frame **(See Figure 5, element 505)**; writing blocks of the demultiplexed data frame at the first size into a register **(Figure 5, blocks of 32 bits are written in data transfer registers 510)**; reading blocks of a second size, different from the first size, from the register **(Figure 5, Blocks of 64 bits are read from data registers 510)**; and multiplexing the blocks **(Figure 5, element 511)** to form an output data frame of the second size. **(Blocks of 64 bits are formed as an output of Figure 5, element 511 – See also Column 5:5-55)**

8. Regarding **claims 2, 10, and 15**, Kincaid teaches a method and device wherein receiving a data frame of a first size includes receiving a 64-bit data frame at the demultiplexer and the multiplexer outputs a data frame of 66-bits. **(Kincaid discloses in Column 2:46-50 that the received input signal can be any size. He indicates converting a block of 32 bits to a block of 64 bits is an example and his method is applicable to converting block size to accommodate data transfer between two buses having two different speeds including 64-bits and 66-bits data buses.)**

9. Regarding **claim 17**, Kincaid teaches a device using a multiplexer as shown in Figure 5. **(In the discussions in Column 2:46-50 it is clear that Kincaid's system can accommodate different frame formats and to accomplish such a task it is inherent to use various types of multiplexers including 32:1 muxs. Examiner takes Official Notice in indicating that use of a thirty-two to one multiplexer is well**

**known as indicated for instance in Tomar et al (US 6, 944, 190) in Figure 10 and Column 13:50-67.)**

10. Regarding **claim 12**, Kincaid discloses a device that includes a first counter **(Figure 5, element 506)** to control the writing of data from the demultiplexer to the register.

11. Regarding **claim 13**, Kincaid discloses a device that includes a second counter **(Figure 5, element 508)** to control the reading of data from the register to the multiplexer.

12. Regarding **claim 19**, Kincaid discloses a device wherein the multiplexer reads data from the register in 66-bit blocks. **(This can easily be accommodated by Kincaid 's system when implementing it as a system for transferring data between a 64-bits wide data bus and a 66-bits wide data bus)**

13. Regarding **claim 20**, Kincaid discloses a device wherein the demultiplexer **(See Figure 5, element 505)** writes data in blocks of a first size **(See Figure 5, block size of 32 bits)** to the register **(See Figure 5, element 510)** and the multiplexer **(Figure 5, element 511)** reads data in blocks of a second size **(Figure 5, Block size of 64 bits)**, different from the first size from the register.

14. **Claims 1, 11, 21, and 22** are rejected under 35 U.S.C. 102(e) as being anticipated by Walker et al (US Pub. No. 2004/0228364), hereinafter referred to as Walker.

*Walker like Kincaid teaches system and method for data transfer between buses having different speeds.*

15. Regarding **claims 1 and 11**, Walker discloses a method and device comprising: receiving a data frame of a first size **(Figure 8B, element 310 receiving a data frame of size 32 bits (i.e. quad) and last line in Paragraph 133)**; demultiplexing the data frame **(Figure 8B, elements 303, 311, 312 – demultiplexed into blocks 32 bits)**; writing blocks of the demultiplexed data frame at the first size into a register **(Figure 8B, elements 311, 312 and 304)**; reading blocks of a second size **(Figure 8B, elements 313 and 304 – blocks of 64 bits)**, different from the first size **(Figure 8B, element 311, 32 bits)**, from the register **(Figure 8B, element 304)**; and multiplexing the blocks to form an output data frame of the second size **(Figure 8B, element 308 is the assembler and is shown to contain a multiplexer in Figure 1, element 34 as discussed in Paragraphs 142.) (See also Paragraphs 133 to 142 for a detailed discussion.) (Examiner wants to point out that the Applicant in the Remarks, page 10, and paragraph 5 of the amendment filed on 2/8/2006 indicated that in Walker's system there is nothing that indicated the size of the blocks written into register 304 is different from the size of the blocks read from register 304. Walker clearly indicates in paragraphs 41 and 134 the input to the register 304 is a quad (i.e. block of eight words or 32 bits) and in paragraph 135, lines 4-6, clearly shows what is read out of the register is formed from a pair of quads (i.e. a block of 64-bits)**

16. Regarding **claim 21**, Walker discloses a device wherein the device is part of a physical coding sub layer. **(See Paragraph 33 and Figure 1, element 14)**

17. Regarding **claim 22,** Walker discloses a device wherein the device is part of a receiver in a fiber optic network. **(See Paragraph 49)**

18. **Claims 23-26 and 33** are rejected under 35 U.S.C. 102(e) as being anticipated by Sriram (US 6, 331, 976).

*Sriram discloses a system and method for synchronization word detection in bit stream communications apparatus.*

19. Regarding **claim 23,** Sriram discloses a method comprising: receiving a stream of data **(Column 2, Lines 33-35 and Column 7, Lines 28-30, and Figure 4C)**; defining a window of a predetermined size within the stream **(Column 6, Lines 65-67)**; examining the window to determine whether at least one synchronization bit is located within the data in the window **(Column 7, Lines 14-17)**; and shifting the window along the stream if a valid synchronization bit is not found in the window **(Column 7, Lines 30-37). (See also Column 3, Lines 5-13 and Figures 4B and 4C)**

20. Regarding **claim 24**, Sriram discloses a method including shifting the window by a predetermined number of bits and filling the opening created by shifting with a bit from a previous cycle. **(See Column 7, Lines 28-43 and Figures 4B and 4C. This is inherent for any window of size L where L > 1)**

21. Regarding **claim 25**, Sriram discloses a method of including storing bits from each successive cycle and providing bits from previous cycles to fill openings created by shifting in subsequent cycles. **(See Column 7, Lines 28-43 and Figures 4B and 4C. This is inherent for any window of size L where L > 1)**

22. Regarding **claim 26**, Sriram discloses a method including successively shifting the window by one bit along the stream of data until valid synchronization bits are located. **(See Column 7, Lines 28-43 and Figures 4B and 4C. This is inherent for any window of size L where L > 1)**

23. Regarding **Claim 33**, Sriram discloses a device **(See Figure 5)** comprising: a first storage element to receive a stream of data **(Figure 5, element 24)**; an element to define a window of a predetermined size within the stream **(Figure 5, element 22)**; a detector to examine the window to determine whether at least one synchronization bit is located within the data in the window **(Figure 5, element 26)**; and a component to shift data along the stream into the window if a valid synchronization bit is not found in the window **(Figure 5, element 24 shows shifting and a shifting mechanism or component is inherent .)**

24. **Claims 23-26 and 33** are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al (US 2002/0015533 A1), hereinafter referred to as Nakamura.

*Nakamura discloses a variable length encoding and decoding apparatus with the ability to detect the synchronizing word/bit in a bit stream.*

25. Regarding **claim 23,** Nakamura discloses a method comprising: receiving a stream of data **(Figure 1, data Do and see also paragraphs 38 and 40)**; defining a window of a predetermined size within the stream **(Figure 1, Register 100 and See paragraphs 40 and 41)**; examining the window to determine whether at least one synchronization bit is located within the data in the window **(Figure 1, element 119 and paragraph 53)**; and shifting the window along the stream if a valid synchronization bit is

not found in the window **(See Paragraphs 65 and 66 and Figure 2, steps 205 and 207)**

26. Regarding **claim 24**, Nakamura discloses a method including shifting the window by a predetermined number of bits and filling the opening created by shifting with a bit from a previous cycle. **(See Paragraph 11, Lines 1-7)**

27. Regarding **claim 25**, Nakamura discloses a method of including storing bits from each successive cycle and providing bits from previous cycles to fill openings created by shifting in subsequent cycles. **(See Paragraphs 11, Lines 7-13 and Paragraphs 42-44)**

28. Regarding **claim 26**, Nakamura discloses a method including successively shifting the window by one bit along the stream of data until valid synchronization bits are located. **(See Paragraphs 22 and 65-67)**

29. Regarding **claim 33**, Nakamura discloses a device **(See Figure 1)** comprising: a first storage element to receive a stream of data **(Figure 1, Register 100 and Paragraph 40)**; an element to define a window of a predetermined size within the stream **(Figure 1, Register 104)**; a detector to examine the window to determine whether at least one synchronization bit is located within the data in the window **(Figure 1, element 119)**; and a component to shift data along the stream into the window if a valid synchronization bit is not found in the window **(Figure 2, steps 205 and 207; Paragraphs 22 and 65-67)**

***Claim Rejections - 35 USC § 103***

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. **Claims 3 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Chen (US 4, 121, 217).

Kincaid teaches all aspects of the claimed invention as set forth in the rejections of claims 2 and 11 respectively but fails to expressly teach the use of a one to thirty-three demultiplexer.

*Chen teaches various interface units for data transmission networks.*

Chen teaches the use of one to thirty-three demultiplexer. **(See Figure 13, element 252)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kincaid's apparatus to incorporate the use of one to thirty-three demultiplexer, the motivation being it would allow his system to combine and separate telecom pipes that carry 32 channels such as E1 pipes with ease and added flexibility.

32. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Chen as applied to claim 3 above, and further in view of Ryan (US 6, 560, 669).

33. Regarding **claim 4**, the combination of Kincaid and Chen teaches all aspects of the claimed invention as set forth in the rejections of claim 3 but fails to teach expressly writing blocks of 64 bits into memory.

*Ryan teaches a method and apparatus for performing a block write to a memory device.*

Ryan discloses writing blocks of 64 bits into memory. **(See Figure 10, elements 130 and 124 and also Column 7, Lines 5-20)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Kincaid's and Chen's apparatus to incorporate writing blocks of 64 bits into memory, the motivation being in the telecom world a frame of size 64 bits is common for ISDN BRI and PRI systems as well as systems based on DSLs and Kincaid's system would be required to support these applications as his system supports any protocol.

34. Regarding **claim 5**, Kincaid discloses a method wherein writing the blocks into a register include writing 2,112 bits into a register. **(Determining memory size is a design choice. The Court has rendered a decision indicating that change in size is a design decision In re Rose, 105 USPQ 237 (CCPA 1955) and specifically states the following in the decision: "...We do not feel that this limitation is patentably significant since at most relates to the size of the article under consideration which is not ordinarily a matter of invention.")**

35. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Ryan (US 6, 560, 669).

Kincaid teaches all aspects of the claimed invention as set forth in the rejections of claim 11 but fails to teach writing blocks of 64 bits into memory.

Ryan discloses writing blocks of 64 bits into memory. **(See Figure 10, elements 130 and 124 and also Column 7, Lines 5-20)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kincaid's apparatus to incorporate writing blocks of 64 bits into memory, the motivation being in the telecom world a frame of size 64 bits is common for ISDN BRI and PRI systems as well as systems based on DSLs and Kincaid's system would be required to support these applications as his system supports any protocol.

36. **Claims 6-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Chen and Ryan as applied to claim 5 above, and further in view of Agere (Agere Systems, "10 Gigabit Ethernet PCS Intellectual Property Cores", Preliminary Data Sheet, July 2001).

37. Regarding **claim 6**, the combination of Kincaid, Chen, and Ryan teaches all aspects of the claimed invention as set forth in the rejections of claim 5 but fails to teach controlling a write pointer at a frequency of approximately 161 MegaHertz.

*Agere provides data sheet for a product called ORLI10G.*

Agere discloses a method including controlling a write pointer at a frequency of approximately 161 MegaHertz. **(See Figure 1, RxPLL writing at 161 MHz)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Kincaid's, Chen's and Ryan's apparatus to incorporate a method including controlling a write pointer at a frequency of approximately 161 MHz, the motivation being using a write pointer at such a rate allows the system to write data in the buffer at a slower rate than the incoming rate and consequently helps in minimizing data loss.

38. Regarding **claim 7**, Kincaid discloses a method wherein reading blocks of the second size includes reading blocks of sixty-six bits from the register. **(This is a consequence of trying to convert t format acceptable by a 66-bits wide bus of which Kincaid is capable of handling as stated in Column 2:46-51)**

39. Regarding **claim 8**, Kincaid discloses a method including controlling a read pointer at a frequency of approximately 156 MegaHertz. **(This is strictly a design issue but is already disclosed by Agere in Figure 1 reading at 156.25 MHz and on page 3 in the section describing the gearbox.)**

40. Regarding **claim 9**, Kincaid discloses a method of wherein multiplexing the blocks to form an output data frame of a second size includes forming an output data frame by using a thirty-two to one multiplexer. **(Determining multiplexer size is a design choice. The Court has rendered a decision indicating that change in size is a design decision In re Rose, 105 USPQ 237 (CCPA 1955) and specifically states the following in the decision: "...We do not feel that this limitation is patentably significant since at most relates to the size of the article under consideration which is not ordinarily a matter of invention." Examiner also takes**

**Official Notice in indicating that use of a thirty-two to one multiplexer is well known as indicated for instance in Tomar et al (US 6, 944, 190) in Figure 10 and Column 13, Lines 50-67.)**

41. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Agere (Agere Systems, "10 Gigabit Ethernet PCS Intellectual Property Cores", Preliminary Data Sheet, July 2001).

Kincaid fails to teach controlling a write pointer at a frequency of approximately 161 MHz and reading at 156 MHz.

Agere discloses a method including controlling a write pointer at a frequency of approximately 161 MHz and reading at 156 MHz. **(See Figure 1, RxPLL2 writing at 161 MHz and Gearbox reading at 156.25 Mhz from RxPLL and on page 3 in the section describing the gearbox.)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kincaid's apparatus to incorporate a method including controlling a write pointer at a frequency of approximately 161 MHz and reading at approximately 156 MHz, the motivation being using a write pointer at such a rate allows the system to write data in the buffer at a slower rate than the incoming rate and consequently helps in minimizing data loss.

33. **Claim 27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Agere (Agere Systems, "10 Gigabit Ethernet PCS Intellectual Property Cores", Preliminary Data Sheet, July 2001).

Sriram teaches all aspects of the claimed invention as set forth in the rejections of claim 23 but fails to teach a pair of synchronization bits in a 66-bit data frame.

Agere discloses a pair of synchronization bits in a 66-bit data frame. **(See Page 4, Lines 1-2 and Figure 3)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Sriram's apparatus to incorporate a pair of synchronization bits in a 66-bit data frame. The motivation being it makes it operable with the widely used Agere's 10-Gigabit Line Interface.

42. **Claims 28 and 30-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Iwanczuk et al (US 6, 323, 681), hereinafter referred to as Iwanczuk.

*Iwanczuk discloses circuits and methods for operating a multiplexer array.*

43. Regarding **claims 28 and 30**, Sriram teaches all aspects of the claimed invention as set forth in the rejection of claim 23 but fails to disclose a method that includes receiving a block of data of the predetermined size in a multiplexer and multiplexing the data into a register.

Iwanczuk discloses a method that includes receiving a block of data of the predetermined size in a multiplexer and multiplexing the data into a register. **(See Figures 5, 7 and 17)**

44. Regarding **claims 31 and 32**, Sriram teaches all aspects of the claimed invention as set forth in the rejection of claim 23 but fails to disclose use of array of multiplexers in detecting synchronization patterns.

Iwanczuk discloses use of array of multiplexers in detecting synchronization patterns. **(See Figure 17, element 71)**

45. With respect to **claims 28 and 30-32**, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Sriram's apparatus to incorporate a method of receiving a block of data of the predetermined size in an array of multiplexer and multiplexing the data into a register. The motivation being it makes it easy for the system to exploit a wider data bus by using an array of multiplexers multiplexing data into a register as discussed in the abstract and back ground section of Iwanczuk's disclosure.

46. **Claims 34-42** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Iwanczuk and Renz.

47. Regarding **claims 34, 40, and 41**, Sriram teaches all aspects of the claimed invention as set forth in the rejection of claim 33 including a control to determine whether or not valid synchronization bits have been located in a series of data frames **(See Figure 5, element 36 – some form of controller to control the shifting is inherent)**.

Sriram fails to disclose a device including a multiplexer coupled to the data stream and the first storage element to receive data; a second storage element coupled to the output of the multiplexer to receive a data frame.

Iwanczuk discloses a device including a multiplexer **(Figure 17, 73)** coupled to the data stream and the first storage element **(Figure 17, 72)** to receive data; a second

storage element **(Figure 17, 74)** coupled to the output of the multiplexer to receive a data frame.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Sriram's apparatus to incorporate a method of receiving a block of data of the predetermined size in a multiplexer from a 1st storage element and multiplexing the data into a 2nd storage element. The motivation being it makes it easy for the system to exploit a wider data bus by using a multiplexer for multiplexing data into a register as discussed in the abstract and back ground section of Iwanczuk's disclosure.

Sriram fails to disclose the use of a gate in determining synchronization pattern. Sriram also fails to disclose the gate can be an exclusive or gate.

*Renz teaches a method and circuitry for detecting synchronization of two words between a measurement signal and a reference signal.*

Renz discloses the use of a gate in determining synchronization pattern. Renz also discloses the gate can be an exclusive or gate. **(See Figure 3, element 9 and also Column 3, Lines 25-35)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Sriram's apparatus to incorporate the use of a gate in determining synchronization pattern. The motivation being the use of gates like exclusive or is easier from a hardware implementation aspect given that for both high and low match it outputs a low signal as indicated in Renz Column 4, Lines 28-31.

48. Regarding **claims 35 and 36**, Sriram fails to expressly disclose a device wherein the control is a state machine that controls the counters (i.e. registers) that control the operation of the multiplexer.

Iwanczuk discloses a device wherein the control is a state machine that controls the counters (i.e. registers) that control the operation of the multiplexer. **(See Tables 5 and 8)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Sriram's apparatus to incorporate the use of state machine for controlling the operation of the multiplexer. The motivation being the use of finite state machine simplifies the type of code being written to control the hardware by defining a single error state and allowing all error handling code to be consolidated in this state.

49. Regarding **claim 37**, Sriram discloses a device of wherein the first and second registers are sixty-six bit registers. **(Determining register size is a design choice. The registers in Figure 5 can be any size. The Court has rendered a decision indicating that change in size is a design decision In re Rose, 105 USPQ 237 (CCPA 1955) and specifically states the following in the decision: "...We do not feel that this limitation is patentably significant since at most relates to the size of the article under consideration which is not ordinarily a matter of invention.")**

50. Regarding **claim 38**, the combination of Sriram and Iwanczuk teaches a device using a multiplexer as shown in Figures 9 and 17. **(It is clear that the combination of Sriram's and Iwanczuk's system can accommodate different frame formats and to**

**accomplish such a task it is inherent to use various types of multiplexers including 66:1 muxs. Examiner takes Official Notice in indicating that use of a sixty-six to one multiplexer is well known in the art as indicated for instance in Cook et al (US Pub. No. 20040078740) in Figure 5 and Paragraph 62.)**

51. Regarding **claim 39**, Sriram discloses a device wherein the multiplexer receives sixty-six shifts. **(Column 7, Lines 1-26)**

52. Regarding **claim 42**, Sriram discloses a device wherein the first storage element stores bits from each successive cycle and provides bits from previous cycles to fill openings created by shifting in subsequent cycles. **(See Column 7, Lines 28-43 and Figures 4B and 4C. This is inherent for any window of size L where L > 1)**

53. **Claim 43** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Iwanczuk as applied to claim 42 above, and further in view of O'Connor et al (US 5, 010, 559).

The combination of Sriram and Iwanczuk teaches all aspects of the claimed invention as set forth in the rejections of claim 42 but fails to teach a device of including a counter that receives a signal from the control and issues a signal to the multiplexer to shift a window of data output by the multiplexer along the serial data stream.

*O'Connor teaches a method and apparatus for synchronizing data frames in a serial bit stream.*

O'Connor discloses a device including a counter that receives a signal from the control and issues a signal to the multiplexer to shift a window of data output by the

multiplexer along the serial data stream. **(See Figure 5 and discussion in Column 5, Lines 35-50)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Sriram and Iwanczuk apparatus to incorporate the use of a device including a counter that receives a signal from the control and issues a signal to the multiplexer to shift a window of data output by the multiplexer along the serial data stream. The motivation being such a device can easily be designed and is simple enough to implement as part of an integrated circuit as indicated in O'Connor Column 2, Lines 55-60.

54. **Claims 44-49** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Iwanczuk.

55. Regarding **claims 44-47**, Sriram fails to disclose a device wherein the first storage element includes an array of multiplexers arranged in rows and columns wherein each row of multiplexers provides one window of data. Further Sriram fails to disclose a device wherein a second array of multiplexers coupled to the first array of multiplexers and that also includes a register that receives the output from the second array of multiplexers.

Iwanczuk discloses a device wherein the first storage element includes an array of multiplexers arranged in rows and columns wherein each row of multiplexers provides one window of data **(See Figure 9, element 62 and Column 12, Lines 60-67).** Further Iwanczuk discloses a device wherein a second array of multiplexers coupled to the first array of multiplexers and that also includes a register that receives

the output from the second array of multiplexers.**(See Figure 17, Column 21, Lines 10-17)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Sriram's apparatus to incorporate a device wherein the first storage element includes an array of multiplexers arranged in rows and columns wherein each row of multiplexers provides one window of data and wherein a second array of multiplexers are coupled to the first array of multiplexers and that also includes a register that receives the output from the second array of multiplexers. The motivation being it makes it easy for the system to exploit a wider data bus by using an array of multiplexers multiplexing data into a register as discussed in the abstract and back ground section of Iwanczuk's disclosure.

56. Regarding **claim 48**, Sriram discloses a device including a gate to determine whether or not at least one bit in the register is a synchronization bit. **(See Figure 5 elements 24 and 26 where an AND operation is done bit by bit)**

57. Regarding **claim 49**, Sriram discloses a device that includes a state machine coupled to the output of the gate. **(See Column 7, Lines 50-67)**

58. **Claims 29 and 50-52** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Iwanczuk as applied to claims 28 and 49 above, and further in view of Renz (US 5, 430, 746).

59. **Regarding claims 29, 50, and 51**, the combination of Sriram and Iwanczuk teaches all aspects of the claimed invention as set forth in the rejection of claims 28 and

49 but does not disclose the use of exclusive or gate in determining synchronization pattern and a state machine is coupled to the output of the gate.

Renz discloses the use of exclusive or gate in determining synchronization pattern and a state machine is coupled to the output of the gate. **(See Figure 3, element 9 and also Column 3, Lines 25-35)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Sriram's and Iwanczuk's apparatus to incorporate the use of exclusive or gate coupled with a state machine in determining synchronization pattern. The motivation being the use of an exclusive or gate is easier from a hardware implementation aspect given that for both high and low match it outputs a low signal as indicated in Renz Column 4, Lines 28-31.

60. Regarding **claim 52**, the combination of Sriram and Iwanczuk teaches all aspects of the claimed invention as set forth in the rejection of claims 44 and 49 including a counter coupled to the state machine and the first array of multiplexers to select a row of multiplexers in the first array. **(See Iwanczuk's Figure 17)**

61. **Claims 53-55** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Iwanczuk and Renz as applied to claim 51 above, and further in view of Agere (Agere Systems, "10 Gigabit Ethernet PCS Intellectual Property Cores", Preliminary Data Sheet, July 2001).

The combination of Sriram, Iwanczuk, and Renz teaches all aspects of the claimed invention as set forth in the rejection of claims 51but fails to disclose a device

including a gear box to convert 64-bit data frames to 66-bit data frames and a physical coding sublayer and also being a receiver for a fiber optic network.

Agere discloses a device including a gear box to convert 64-bit data frames to 66-bit data frames **(See Figure 1 and 1st paragraph on page 3)** and a physical coding sublayer **(See Figure 5)** and also being a receiver for a fiber optic network **(See Page 3 uses optical XSBI interface can be part of the transmit or receive circuit.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Sriram's, Iwanczuk's, and Renz's apparatus to incorporate a device including a gear box to convert 64-bit data frames to 66-bit data frames and a physical coding sublayer and also being a receiver for a fiber optic network. The motivation being it makes it compliant to the IEEE 802.3ae Standard and broadens the applicability of the device in different types of networks including optical network.

***Response to Arguments***

62. Applicant's arguments with respect to claims 1 and 11-13 have been considered but are moot in view of the new ground(s) of rejection.

63. In the Remarks, with respect to claims 31, 32, 44, and 45, Applicant argues that Iwanczuk fails to teach an array of multiplexers as specifically claimed in claims 31, 32, 44, and 45. Applicant further asserts that Iwanczuk's Figure 9, which was cited for showing an array of multiplexers by the Examiner in the last Office Action, fails to show multiplexers arranged in rows and columns wherein each row of multiplexers provides one window of data. Examine respectfully disagrees with Applicant's conclusions.

Iwanczuk teaches an array of multiplexers and Iwanczuk's Figure 9 shows multiplexers arranged in rows and columns. First as a matter of definition an array can contain one row and many columns and based on such definition Figure 9 indeed shows an array of multiplexers. Further, Iwanczuk's shows in Column 12:60-67 that each of the 16:9 multiplexers in Figure 9 consist of 8:1 multiplexers effectively constituting the rows and columns of the multiplexer array 62 of Figure 9. Figures 10 A, B, C are circuit diagrams of multiplexers that make up the multiplexer array of Fig. 9 as indicated in Columns 4:53-55 and 13:45-67. Finally each multiplexer in the multiplexer array of Figure 9 receives a portion of the data stream from the registers effectively placing a window of data from the data contained in the registers as shown in Table 2. The Applicant has not shown why Iwanczuk's array of multiplexers is different from that of the Applicant's invention and it is the position of the Examiner that there is no structural difference between Iwanczuk's and Applicant's array of multiplexers.

64. Finally, the Examiner wants to emphasize that the current Application addresses two distinct inventions. Namely, the first invention is a method of converting frame sizes in order to accomplish communication between two data buses with different widths and the second invention deals with detecting synchronization bits in a data stream. The first invention and corresponding claims 1-20 is clearly anticipated by the teachings of Kincaid. In addition to Kincaid, Walker also anticipates the first invention. Sriram and Nakamura also anticipate the independent claims 23 and 33 of the second invention. Further the Examiner has listed some of the prior arts that can read on independent claims 23 and 33 as the technique of detecting synchronization bits by using shift

registers and logic gates is well known in the art. The Examiner also wants to emphasize that Iwanczuk teaches array of multiplexers in an environment data frame size is converted to accommodate communication between incompatible buses (i.e. buses with different widths) as indicated in Iwanczuk's Columns 3:12-18 and 11:18-23 and Figure 7.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following adequately anticipate claims 23 and 33 that deal with means to detect synchronization bits using shift registers and logic gates:

US Patent (6, 275, 552) to Ando

US Patent (4, 748, 623) to Fujimoto

US Patent (5, 018, 140) to Lee et al

US Patent (4, 404, 675) to Karchevski

US Patent (6, 163, 423) to Lee et al

US Pub. No. (2002/0110208 A1) to Suzuki

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Habte Mered
12-8-2006

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